This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Currently Amended) A method for fabricating a transistor in a semiconductor device, comprising:

forming an isolation region in a semiconductor substrate and sequentially depositing a pad oxide layer, a pad nitride layer and a first oxide layer on the substrate and the isolation region ;

~~patteringpatterning~~ the first oxide layer and the pad nitride layer to form a gate electrode opening;

depositing a doped poly silicon layer over the whole semiconductor substrate including the opening;

~~forming a doped polysilicon sidewall on the pad nitride layer and the first oxide layer~~etching back the doped poly silicon layer until the pad oxide layer is exposed to form a doped polysilicon sidewall on a sidewall of the pad nitride layer and the first oxide layer, wherein the doped polysilicon sidewall is used to serve as the lightly doped drain (LDD) implantation;

etching the pad oxide layer exposed by the doped polysilicon sidewall to expose the semiconductor substrate;

forming a gate isolation layer on the exposed semiconductor substrate;

sequentially depositing and planarizing ~~a gate isolation layer,~~ a gate nitride layer covering the gate isolation layer and the doped polysilicon sidewall, and a metal layer on the whole substrate to form the gate electrode; and

forming a source, a drain, a gate plug, a source plug and a drain plug, respectively.

2. (Original) The method of claim 1, wherein the isolation region is shallow trench isolation(STI).

3. (Original) The method of claim 1, wherein a thickness of the pad oxide layer is not less than 50 angstrom.

4. (Currently Amended) The method of claim 1, wherein a local channel ion implantation is performed ~~only in case a source and a drain region is salicidated or a lightly doped drain (LDD) implantation is performed before depositing the gate isolation layer~~ before depositing the gate isolation layer if the source or drain region have an increased resistance.

5. (Cancelled)

6. (Original) The method of claim 1, wherein the gate nitride layer is made of at least one of TiN and TaN.

7. (Original) The method of claim 1, wherein the metal layer is made of tungsten (W).

8. (Original) The method of claim 2, wherein the thickness of the pad oxide layer under the doped poly silicon sidewall is controlled to be used to serve as the LDD implantation.